Wafer-scale nanofabrication of sub-100 nm arrays by deep-UV displacement Talbot lithography

OPEN ACCESS
IOP Publishing
Nanotechnology

Nanotechnology **31** (2020) 295301 (9pp)
https://doi.org/10.1088/1361-6528/ab8764

Wafer-scale nanofabrication of sub-100 nm arrays by deep-UV displacement Talbot lithography

Víctor J Gómez, Mariusz Graczyk, Reza Jafari Jam, Sebastian Lehmann and Ivan Maximov

Division of Solid State Physics and NanoLund, Lund University, Box 118, SE - 211 00, Lund, Sweden

E-mail: victor.gomez@ftf.lth.se

Received 29 November 2019, revised 22 February 2020
Accepted for publication 7 April 2020
Published 5 May 2020

Abstract

In this manuscript, we demonstrate the potential of replacing the standard bottom anti-reflective coating (BARC) with a polymethylglutarimide (PMGI) layer for wafer-scale nanofabrication by means of deep-UV displacement talbot lithography (DTL). PMGI is functioning as a developable non-UV sensitive bottom anti-reflective coating (DBARC). After introducing the fabrication process using a standard BARC-based coating and the novel PMGI-based one, the DTL nanopatterning capabilities for both coatings are compared by means of the fabrication of etched nanoholes in a dielectric layer and metal nanodots made by lift-off. Improvement of DTL capabilities are attributed to a reduction of process complexity by avoiding the use of O_2 plasma etching of the BARC layer. We show the capacity of this approach to produce nanoholes or nanodots with diameters ranging from 95 to 200 nm at a wafer-scale using only one mask and a proper exposing dose. The minimum diameter of the nanoholes is reduced from 118 to 95 nm when using the PMGI-based coating instead of the BARC-based one. The possibilities opened by the PMGI-based coating are illustrated by the successful fabrication of an array of nanoholes with sub-100 nm diameter for GaAs nanowire growth on a 2″ GaAs wafer, a 2″ nanoimprint lithography (NIL) master stamp, and an array of Au nanodots made by lift-off on a 4″ silica wafer. Therefore, DTL possess the potential for wafer-scale manufacturing of nano-engineered materials.

Supplementary material for this article is available online

Keywords: Displacement Talbot lithography, nanofabrication, sub-100 nm, NW growth template, NIL stamp, Lift-off

(Some figures may appear in colour only in the online journal)

1. Introduction

Nanofabrication of periodic arrays of nanostructures is crucial for the realization of devices controlled down to the nanoscale. Over the last decades there has been a dramatic increase in applications of nanotechnology in fields such as physics, chemistry, biomedicine, and materials science. This leads to the requirement for nanopatterning of large-areas with high reproducibility and throughput at a low cost. There exist a wide variety of patterning techniques, but each one offers different advantages and disadvantages. Deep-ultraviolet immersion lithography, using a 193 nm excimer laser, capable of achieving a resolution of 14 nm, is widely applied in industry [1], and the development of extreme-UV sources will push the resolution further down [2]. However, the associated high costs limit their introduction into companies with a lower volume production and research organisations.

Electron-beam lithography is flexible and able to define features below 10 nm, though, its cost is prohibitive for wafer-scale nanofabrication [3]. Nanoimprint lithography (NIL), based on mechanical pattern transfer between stamp and substrate, is a promising technique for large-area nanopatterning [4–6], able to reach below 10 nm feature size [7]. However, its main disadvantages are the lifetime of the nanoimprint stamp, the need of a flat and/or very clean surface, the mass transfer during imprinting process and the limited control over residues thickness. Nanosphere lithography, which relies on the self-assembly of colloidal spheres, is not suitable to full-wafer nanopatterning yet due to poor pattern fidelity [8, 9]. Laser interference lithography [10], based on the interference of two coherent laser beams, can produce periodic nanopatterns down to 20 nm. Although it is suitable for large-area nanopatterning with high-yield, maintaining the light source stability can be rather challenging.

Recently, Talbot lithography, based on the self-imaging effect called Talbot effect, has emerged as an alternative technique for nanopatterning [11–13]. When highly collimated monochromatic light passes through a periodic pattern (grating or array of holes), several diffraction orders are produced and interfere resulting in a self-image of the regular pattern. This self-image is periodically repeated along the axis perpendicular to the mask. The period of the self-image, called the Talbot distance, is given by [14]:

$$D_T = \frac{\lambda}{1 - \sqrt{1 - \lambda^2/p^2}}$$

Where λ is the wavelength of the illumination light and p is the pitch of the periodic pattern. Due to the complexity and spatial distribution of the interference pattern it is difficult to apply directly the Talbot effect for photolithography. However, by introducing a displacement of the substrate relative to the mask, along the perpendicular direction, it is possible to integrate the optical field and solve the above mentioned issues. Thus, resulting in the development of displacement Talbot lithography (DTL) [15].

DTL has been confirmed as an excellent technique for large area nanofabrication of periodic features at a low cost and insensitive to surface bowing [16, 17]. Applications of DTL include metamaterials [18], dielectric and metal mask fabrication for selective area epitaxy, such as III-Ns nanotubes [19] and nanowires [20–22], nanowires made of bottom anti-reflective coating (BARC) [23], nanoimprint stamp fabrication [24], and neuronal network formation [25], and, by moving the substrate in parallel to the mask while exposing, complex features can be realized [26]. The minimum feature size that can be transfer to the substrate depends on the light source wavelength, on the type of feature and on the different etching steps. Whereas dots of 75 nm [24] and holes of 100 nm [14] can be transferred to the resist layers, it is much harder to achieve such small features in the substrate. Up to now, it has been reported a minimum diameter of 90 nm in top-down Si pillars [24] and of 250 nm in holes transferred to GaN [27].

The DUV lithography processes include the use of a BARC layer together with a DUV sensitive resist. The BARC layer minimizes reflection from the substrate, which can ruin the mask self-image. However, these processes need plasma etching to transfer the pattern from the resist down to the underlying substrate [28]. The widening of the nanoholes when transferring from the resist to the substrate can be attributed to lateral etching of the BARC layer. Therefore, a polymer stacking sequence that keeps the feature size during pattern transfer to the substrate is highly desirable.

To avoid the plasma etching of the BARC layer, significant efforts have been devoted to the research on developable BARCs (DBARCs) [29–31]. DBARCs are developer-soluble-polymer based anti-reflective coatings. The majority of the DBARC polymers reported so far can be classified into photosensitive and non-photosensitive. However, DBARC can be influenced by components and process conditions [32]. Toukhy and co-workers [33] demonstrate a first generation of methacrylate based DBARCs with promising results.

In this manuscript we report for the first time the patterning of sub-100 nm holes in a dielectric mask. To do so, we replace the standard BARC layer by a polymethylglutarimide (PMGI) layer. PMGI is an alkaline soluble polymer derived from Polymethyl methacrylate that can work as a non-imageable DBARC with an isotropic dissolution rate in developer, resulting in a direct transfer of the nanopattern during the development step which in turn results in a reduction of the nanohole diameter. In addition, PMGI is a lift-off resist that produces an undercut, so, there is no need of an additional lift-off resist layer (LOR). Thus, also simplifying the lift-off process. After introducing the standard fabrication process using a BARC layer and the novel process employing a PMGI layer, the DTL nanopatterning capabilities for both processes are compared by means of the fabrication of etched nanoholes and metal nanodots made by lift-off. The pattern on the resist are subsequently transferred to a dielectric or metal mask by etching or lift-off, respectively. Therefore, the fabricated dielectric or metal mask can be applied to futher technological processes including top-down etching or nanowire growth. This process is successfully applied to fabricate an array of nanoholes with sub-100 nm diameter for GaAs nanowire growth, a NIL stamp fabrication, and the preparation of an array of lift-off Au nanodots on a silica wafer. Compared to other nanolithography techniques, this approach offers full-wafer scale fabrication of sub-100 nm nanohole arrays in dielectric masks at low cost.

2. Experimental

All studied samples were prepared on commercial (i) SiO_2 on Si (100), (ii) in-house deposited inductively coupled plasma-chemical vapour deposition (ICP-CVD) SiN_x on Si (100) and GaAs $(111)_B$, or (iii) UV-grade 1 mm thick 4″ fused silica wafers manufactured by SiegertWafer, and WaferTech. The SiNx layers were prepared in a MicroSys-200 manufactured by MicroSystems GmbH, Germany. Samples were exposed in our PhableR 100 DUV photolithography system manufactured by Eulitha AG, Switzerland. The system is equipped with a pulsed ArF excimer laser ($\lambda = 193$ nm). The laser pulse frequency can be tuned from 30 to 150 Hz and the single pulse energy from 0.5 to 5.0 mJ. The DTL system is installed in

its own encasement and dedicated HEPA® filters are mounted for particle and amine concentration reduction. Samples were inspected using a SU8010 cold field emission-scanning electron microscope (FE-SEM), Hitachi, Japan, and a Leo 1560 Thermal FE-SEM, Zeiss, Germany. For the diameter calculations of the features the ImageJ® software and a contrast-based algorithm were employed to measure the areas and circularities of the features to subsequently calculate the diameter of the features. Reactive ion etching (RIE) processes were carried out in a table-top Sirus T2 Plus system from Trion Technology, Inc, US. Ozone cleaning was performed in a UV-ozone cleaner UVOH 150 from FHR Anlagenbau GmbH, Germany. Nanowire (NW) growth was performed in a $3 \times 3''$ Close Coupled Showerhead Metal-Organic Vapour Phase Epitaxial (MOVPE) reactor from Aixtron GmbH, Germany. Regarding NIL, an EiTRE 6 NIL system, manufactured by Obducat AB, Sweden, was employed. The antisticking treatment of the NIL master stamps was carried out in a FIJI plasma enhanced atomic layer deposition system manufactured by Veeco Instruments Inc, USA.

We are going to compare two different coatings for DTL namely the BARC-based and the PMGI-based coatings. On one hand, the standard or BARC-based coating comprises a deep-UV (DUV) resist PAR1077S90 or PAR1085S90 (Sumitomo, Japan) and a BARC GenARC 266 (Brewer Science Inc, USA) layer [34]. On the other hand, the PMGI-based process includes the same deep-UV resists and a PMGI SF3S polymer (MicroChem Corp, USA) replacing the BARC layer.

3. Results and discussion

In order to do a fair comparison, both coatings will be employed in the fabrication of etched nanoholes in a dielectric layer and lift-off nanodots.

3.1. Etching process BARC vs. PMGI

The fabrication of arrays of nanoholes is technologically attractive for many different processes, such as the realization of masks for the selective growth of nanostructures such as III–V nanowires [5, 6, 35–37], for the preparation of NIL stamps [24], and the fabrication of porous layers [27] to name a few.

The DTL exposures (figure 1(a)) were performed using a phase shift mask with a hexagonal array of nanoholes of 200 nm diameter with 500 nm pitch. The gap between mask and wafer was set to 80 μm, and the range of displacement was set to aproximately 3 Talbot lengths of $\sim$ 8 μm. Laser pulse energy was set to 1.5 mJ and frequency to 100 Hz and the accumulated dose was varied between 2.5 mJ cm^{-2} and 7.0 mJ cm^{-2}.

The substrates employed for the etching of nanoholes, independent of the coating used, were $2''$ Si(100) with a 100 nm SiO_2 dielectric layer. Figure 1 shows the schematic representation of the nanopatterning via etching for both BARC- and PMGI- based coatings.

For the preparation of the BARC-based coating (figures 1(a)–(e)), the BARC layer, spun at 2500 rpm for 45 s, was baked at 180 °C during 1 min resulting in a 64 nm thick layer. Then the DUV resist was spun on top at 2000 rpm during 45 s and baked at 90 °C during 1 min for a thickness of 115 nm. After the DTL exposure the wafer was baked at 100 °C for 50 s and developed in MF24A for 50 s (figure 1(b)). Then, the pattern was transferred to the BARC layer via O_2 plasma etching (figure 1(c)) at room temperature (RT), 40 sccm O_2, 150 mTorr, and 50 W of radio-frequency (RF) power, resulting in an etch rate of ~54 nm min^{-1}. The pattern created on the BARC layer was transfer further into the dielectric layer (SiO_2 in this case) via reactive ion etching (RIE, figure 1(d)), in the above mentioned Sirus T2 system, with a mixture of 5 sccm CHF_3 and 5 sccm CF_4, at RT, 50 mTorr, and 75 W of RF power, resulting in an etch rate of ~18 nm min^{-1}. Finally, the wafer surface was cleaned from polymers and residues with O_2 plasma (figure 1(e)) at the conditions described for the etching of the BARC layer.

The PMGI-based coating (figures 1(f)–(i)) was prepared according to the following recipe. The wafers were spin-coated with PMGI at 2500 rpm for 45 s, and baked at 200 °C for 10 min resulting in a 75 nm thick layer. Afterwards, the DUV resist was spun on top at 2000 rpm during 45 s and baked at 90 °C for 1 min resulting in a thickness of 115 nm. After the DTL exposure (figure 1(f)) the wafer was baked at 100 °C for 50 s and developed in MF24A for 50 s (figure 1(g)), transferring the pattern directly into the PMGI layer. Then, the pattern created on the PMGI layer was transferred further into the dielectric layer (SiO_2 in this case) via reactive ion etching (RIE, figure 1(h)), in the above mentioned Sirus T2 system, with 10 sccm of CHF_3, at RT, 20 mTorr, and 75 W of RF power, resulting in an etch rate of ~18 nm min^{-1}. In a final step, the wafer surface was cleaned from polymers and residues with ozone (figure 1(i)) at 90 °C, a flow of O_2 of 500 sccm, and a wide band UV irradiation intensity for O_3 generation of 50 mW cm^{-2}.

Figure 2 shows the nanoholes experimentally transferred to the SiO_2 dielectric layer following the process described in figure 1 for both coatings. The patterns were achieved for various accumulated doses in a positive resist with only one mask. The nanohole openings diameter increases from ~118 to ~256 nm for the BARC-based coating (figures 2(a)–(c)) and from ~95 to ~179 nm for the PMGI-based one (figures 2(f)–(h)). For accumulated doses below 2.5 and 3.0 mJ cm^{-2} for BARC and PMGI respectively, defects in the form of vacancies (missing holes) and or underdeveloped nanoholes start to occur. Those problems are related to an inhomogeneous DTL exposure (see SI figure S1 stacks.iop.org/Nano/31/295301/mmedia). On the other hand, for accumulated doses over 5.5 and 7.0 mJ cm^{-2} for BARC and PMGI respectively, additional features surrounding the nanoholes appear. Those features are the result of the second order diffraction pattern that occurs at high enough accumulated doses [14]. It is worth mentioning that the final nanohole size can be controlled not only by the accumulated dose (figure 2), but also by resists thickness optimization (see SI figure S2).

The minimum diameter of the nanoholes is 95 nm and 118 nm by using the PMGI- and the BARC- based coatings respectively, for the defect free exposure conditions (see SI

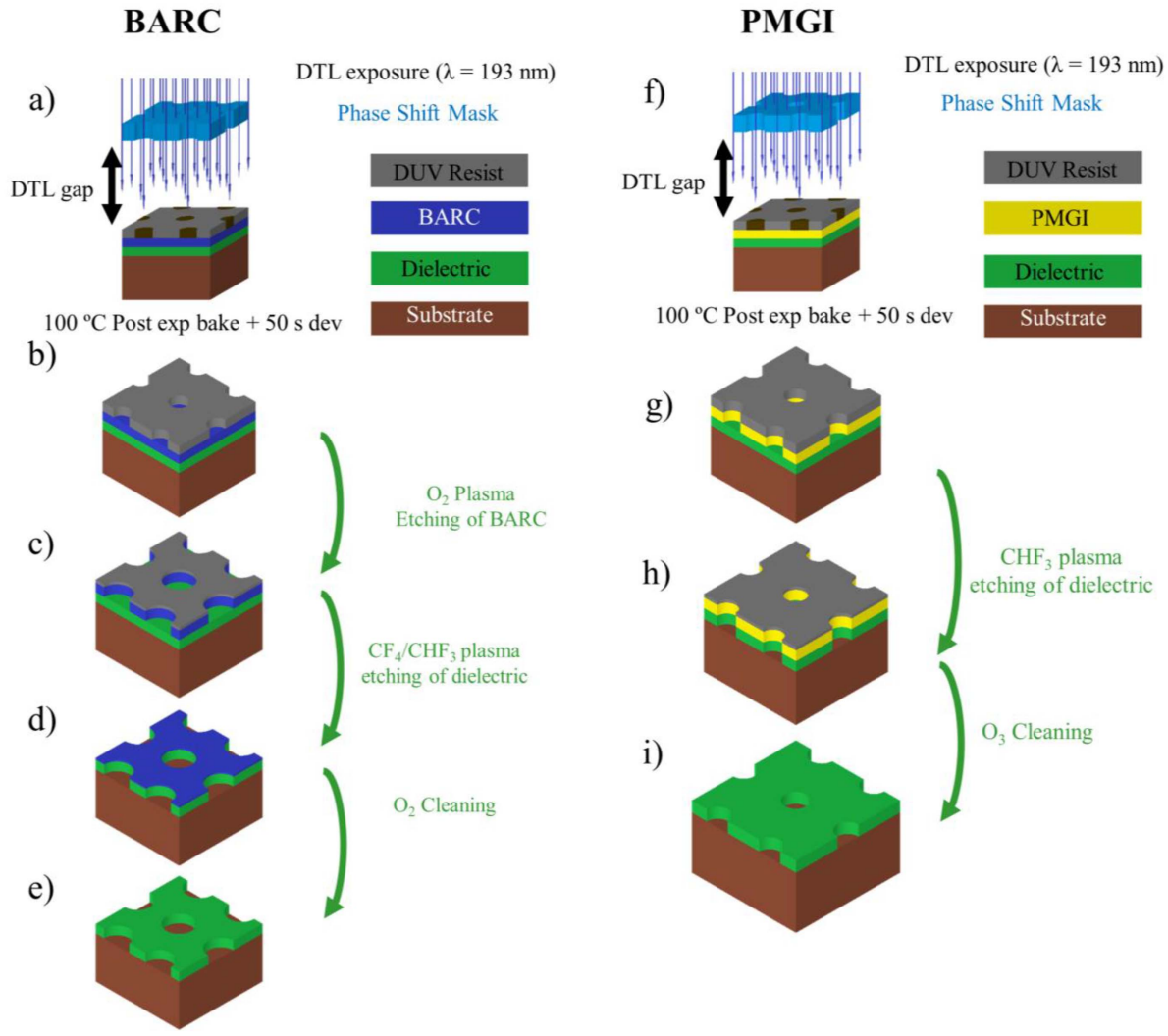

Figure 1. The schematic representation of the nanofabrication process via DTL for the BARC- and PMGI- based coatings. For the BARC-based coating (a) layer stacking sequence, DTL exposure, post-baked at 100 °C, after the exposure (b) the wafer is first developed in MF24A, (c) then the pattern is transferred to the BARC layer via O_2 plasma etching, (d) subsequently transferred again to the dielectric layer via CF_4/CHF_3 dry etching and finally, (e) the wafer is cleaned from polymer residues via O_2 plasma cleaning. For the PMGI-based coating (f) layer stacking sequence, DTL exposure, post-baked at 100 °C, after the exposure (g) the wafer is first developed in MF24A transferring the pattern to the DUV resist and the PMGI polymer, (h) then the pattern is transferred to the dielectric layer via CHF_3 dry etching, and finally (i) the wafer is cleaned from polymer residues via O_3 cleaning.

figures S1 and S2). The main difference between the processes described for both coatings is that in case of the PMGI-coating the pattern is transferred to the PMGI layer during the development step (figure 1(g)), thus, simplifying the process by avoiding the O_2 plasma etching, also known as de-scum, of the BARC layer. In addition, the O_2 plasma etching rate of DUV resist is higher than of BARC layer (see supporting info, SI, figure S3). The absence of selectivity during the de-scum step makes it not suitable for transferring the pattern into the layer beneath, affecting the total thickness of nanopatterned resists (after de-scum DUV resist is almost completely etched) and nanohole edge slope. Therefore, an obvious advantage of replacing the BARC layer by PMGI is the possibility of maintaining the size and shape of the nanoholes, and to create a proper slope for transferring the nanoholes into the underneath dielectric layer. It is worth mentioning that during the etching of the dielectric, the deposition of a CF_x layer on top of the resist protects it against erosion during etching [38], which in turns helps keeping the nanohole edge slope, and the total thickness of the nanopatterned resists. Moreover, the recipe described to etch the nanoholes into the SiO_2 or SiN_x dielectric layer creates a ~78–82° slope that maintains the nanohole size (see SI figure S4) created by using PMGI with respect to the ones obtained with BARC.

In the experiments described in this article, the BARC layer employed (GenARC 266) was insensitive to DUV radiation and insoluble in developer (MF24A), so it was needed the use of an O_2 plasma etching to transfer the nanopattern from the DUV resist to the BARC layer. The poor selectivity between the DUV resist and the BARC layer against

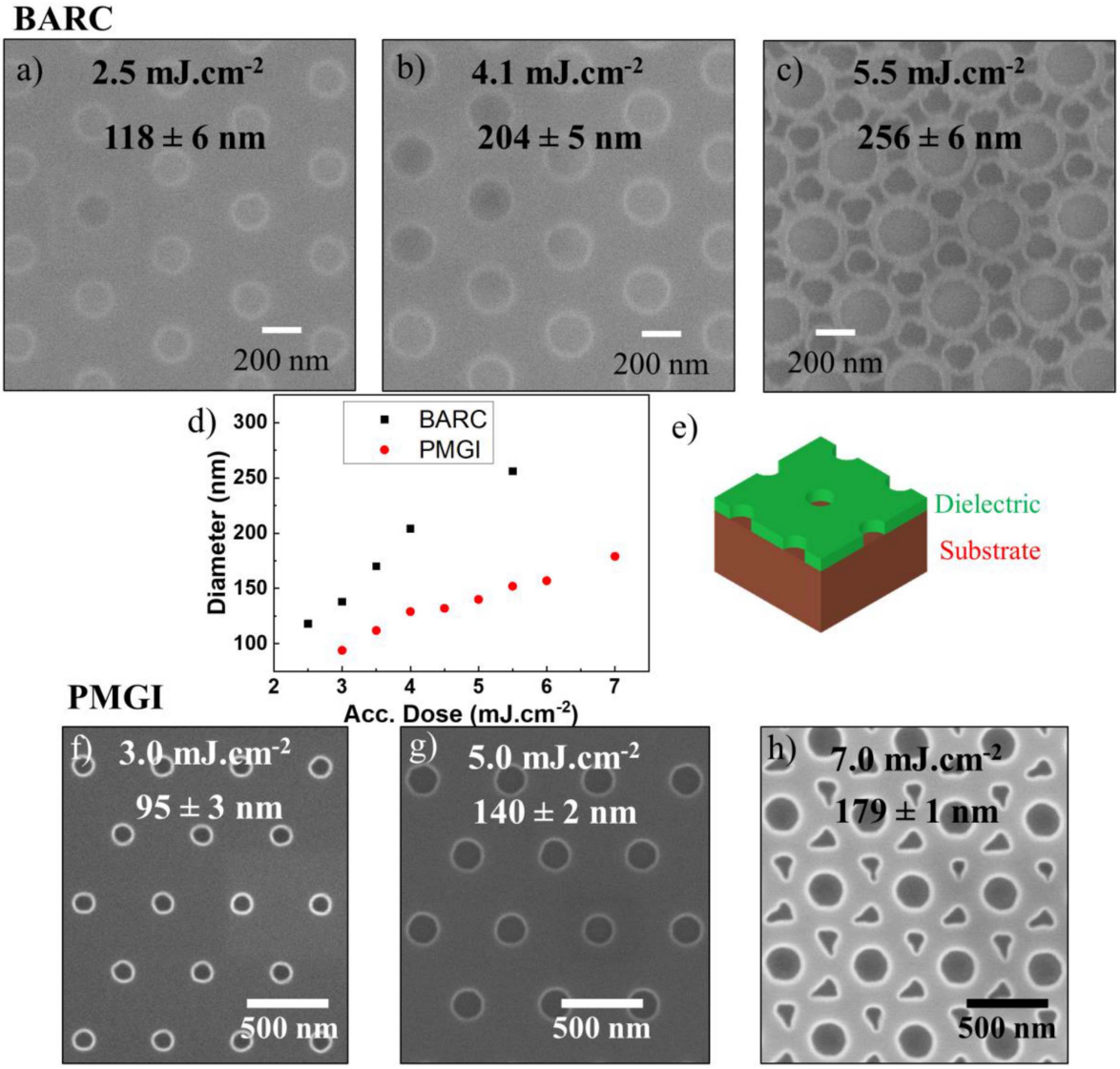

Figure 2. Nanohole patterns transferred to the dielectric layer after the DTL and RIE processes for the BARC-based coating at an accumulated dose of (a) 2.5 mJ cm^{-2}, (b) 4.1 mJ cm^{-2}, and (c) 5.5 mJ cm^{-2}. (d) Diameter of the nanohole openings transferred to the dielectric layer vs the accumulated dose for both, the BARC- and the PMGI- based coatings. (e) Schematic representation of the layer stacking sequence. Nanohole patterns transferred to the dielectric layer after the DTL and RIE processes for the PMGI-based coating at an accumulated dose of (f) 3.0 mJ cm^{-2}, (g) 5.0 mJ cm^{-2}, and (h) 7.0 mJ cm^{-2}.

the O_2 plasma ruins the resist profile making it not suitable for an appropriate nanopattern transference. On the contrary, when using the PMGI-based coating, as the PMGI polymer is soluble in MF24A developer, the O_2 plasma etching can be avoided and the abovementioned detrimental issue can be overcome.

We cannot claim that PMGI is better than BARC generally. For example, UV sensitive BARC, soluble in developer and optimized for 193 nm wavelength can be a challenge in order to give a better resolution.

Regarding the limitations of PMGI, the dissolution rate in the developer strongly depends on baking temperature (200 °C in this case) and on the development time. The dissolution of PMGI in MF24A is isotropic and undercut should be as deep as the PMGI thickness. However, the optimal PMGI thickness is also important due to its antireflective properties. Those are the main limit for the resolution due to the risk of pattern collapse.

Regarding DUV light absorption, PMGI has a relatively high extinction coefficient at 193 nm making it suitable for DTL [39]. In addition, the thickness of the dielectric layer, such as SiO_2 or SiN_x, can be engineered to further reduce reflections from the substrate. Thus, achieving an even better resolution.

In addition, as DTL is a non-contact technique, the fabrication of nanoholes in a dielectric mask does not depend on the surface roughness of the dielectric layer. In contrast, as NIL is a contact technique, surface roughness plays a significant role in the transference of the pattern, which, in the worst case, can lead to serious damage on the wafer, such as cracks or fractures, due to wafer bowing.

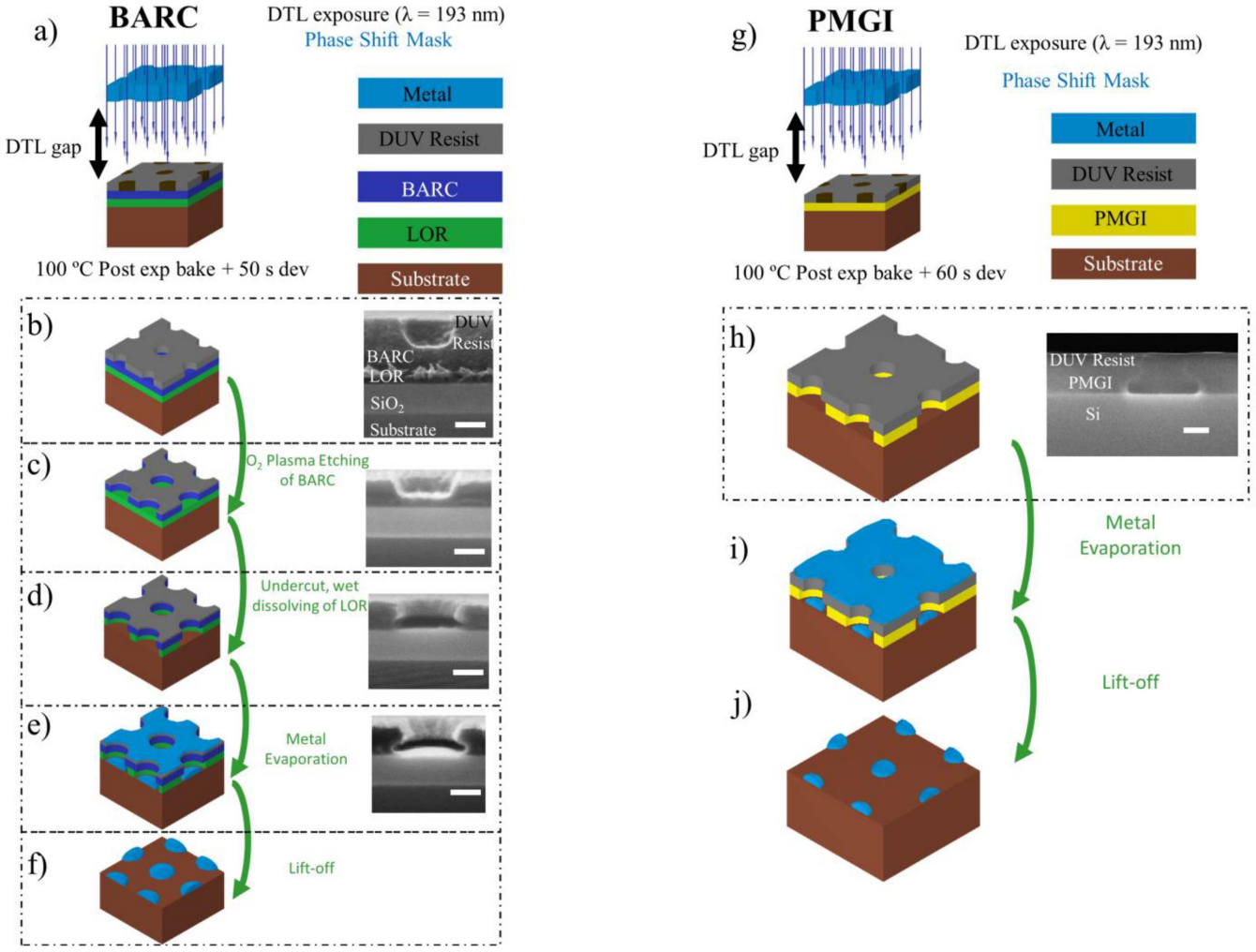

Figure 3. Schematic representation, and the SEM micrographs, of the lift-off nanofabrication process via DTL for the BARC- and PMGI-based coatings. (a) Layer stacking sequence, DTL exposure, post-baked at 100 °C. For the BARC-based coating it is needed the presence of a LOR layer. After the exposure (b) the wafer is first developed in MF24A, (c) then the pattern is transferred to the BARC layer via O_2 plasma etching, (d) undercut formation in the LOR layer, (e) metal evaporation and (f) lift-off. For the PMGI-based coating (g) layer stacking sequence, DTL exposure, post-baked at 100 °C. After the exposure (h) the wafer is first developed in MF24A transferring the pattern to the DUV resist and creating the undercut profile in the PMGI layer, (i) metal evaporation and (j) lift-off. The insets show the cross-section SEM micrographs of the wafer at different steps of the process. The scale bar is 100 nm in all micrographs.

3.2. Lift-off process BARC vs PMGI

Alternatively to the fabrication of nanoholes, metal nanodots can be deposited on the wafer surface by means of lift-off. Figure 3 summarizes the lift-off process for both the BARC- (figures 3(a)–(f)) and PMGI- (figures 3(g)–(j)) based coatings. However, the profile obtained in the BARC layer after the descum process (figure 3(c)) is not suitable for a reliable lift-off due to the lack of undercut profile. Thus, the addition of a lift-off resist (LOR) layer is essential.

The LOR layer was spin-coated on a 100 nm SiO_2/Si wafer at 2500 rpm for 63 s and baked at 200 °C for 10 min resulting on a 70 nm thick LOR layer. After that, the process continued according to the description given in the previous section for the BARC-based coating. After development (figure 3(b)) and O_2 plasma etching (figure 3(c)), the undercut profile was created in a wet etching process (MF319 3:1 H_2O) for 40 s (figure 3(d)). A 20 nm Pt-Pd alloy (80–20 by % weight) was sputtered on the wafer (figure 3(e)). Subsequent lift-off (figure 3(f)) was carried out by soaking the wafer in Microposit Remover 1165 (MicroChem Corp, USA). A clear trend of increasing nanohole diameter size can be recognized after development, O_2 plasma etching and undercut formation (figures 3(b)–(d)).

In the case of the PMGI-based process, a suitable overhanging lift-off profile can be obtained right after the development step (figure 3(h)). It is only necessary to control the development time for an optimised undercut profile; 60 s in figure 3(h). Then, metal was evaporated (figure 3(i)) and lift-off carried out as disscused for the BARC-based process (figure 3(j)).

The use of a PMGI layer significantly reduces the complexity of the fabrication of metal nanodots. A suitable undercut profile can be achieved right after the development

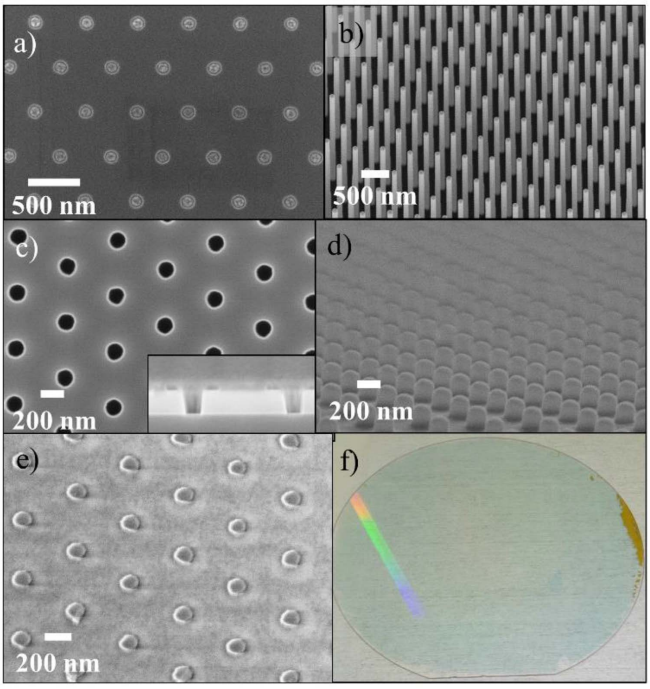

Figure 4. Application of PMGI-based coating to the fabrication of masks for nanowire growth (a) Au nanodots in nanoholes patterned on 2″ 70 nm SiN_x/GaAs $(111)_B$ wafer, (b) Wurtzite-GaAs NWs (diameter of 95 nm); NIL stamps (c) array of nanoholes in 200 nm SiO_2/Si, inset shows cross-section, (d) intermediate polymer stamp fabricated using array shown in (c); (e) lift-off Au nanodots with 140 nm diameter on (f) 4″ fused silica wafer.

of the wafer. In this way, the O_2 plasma etching and its undesirables drawbacks (mentioned in section 3.1) can be avoided.

3.3. Application of PMGI-based process

After describing and comparing the BARC- and PMGI- based coatings, the PMGI-based coating is applied successfully to three different nanofabrication processes (figure 4).

3.3.1. Template for NW growth. Arrays of Au-nanodots inside a nanohole in a dielectric layer conforms a route for pattern preservation in the growth of GaAs NWs via the vapour-liquid-solid (VLS) growth mode [5, 6, 35–37].

A 70 nm thick SiN_x layer was deposited on a 2″ GaAs $(111)_B$ wafer by means of ICP-CVD using a mixture of $Ar/SiH_4/N_2$ (60/10.5/9.5 sccm) at 200 °C, 0.025 mbar and 1000 W ICP power and 3 W RF power, resulting in a deposition rate of 42 nm min^{-1}. Fabrication of nanoholes was performed following the process described in section 3.1 for PMGI-based coating. After completing the fabrication of nanoholes, Au nanodots were electrodeposited (figure 4(a)) using pulsed electrodeposition at a peak current density of 5 mA cm^{-2} (details can be found in SI section 5). Wurtzite-GaAs NWs were grown by means of MOVPE using arsine and trimethylgallium at a V/III ratio of 3.51, and susceptor set temperature of 540 °C for 30 min. Resulting in 2.8 μm long and 95 nm diameter wurtzite GaAs NWs (figure 4(b)). We achieved a 100% yield and pattern preservation, over all scanned areas, due to Au particle locking by the presence of the SiN_x mask. The use of a dielectric mask prevents parasitic growth, as well as facilitates the use of electrodeposited gold to reduce material consumption and to avoid Au residues on the nanohole edges that can contribute to parasitic NW growth.

3.3.2. Fabrication of NIL master stamps. NIL master stamps for a two-step NIL process were fabricated on 2″ 200 nm SiO_2/Si wafers. Fabrication of nanoholes in SiO_2 followed the method described in section 3.1. The mask employed was a phase shift mask with a hexagonal array of nanoholes of 200 nm diameter with 600 nm pitch. The array of nanoholes was transferred to the SiO_2 layer via a CHF_3-based reactive ion etching process using the Si/SiO_2 interface as an etch-stop. Figure 4(c) shows the SEM top-view and the cross-section of the array of nanoholes on the master stamp after the cleaning step. After applying an F-based anti-sticking treatment, the master stamp was replicated into an intermediate polymer stamp, using a soft GMN-PS90 polymer foil. The polymer stamp was prepared in an UV imprint process at room temperature in an Eitre 6 nanoimprinter using a modified version of simultaneous thermal and UV-process (STU) [40]. The polymer stamp (figure 4(d)), which consists of an array of 200 nm tall pillars with a diameter of 170 nm and a pitch of 600 nm, was made as a replica from the DTL-PMGI fabricated 2″ master SiO_2/Si stamp (figure 4(c)). The replicas are defect free with an equal height of pillars over the entire wafer, which is critical for quality and stability of the NIL process on targeted substrates.

3.3.3. Lift-off Au nanodots. Fabrication of arrays of Au nanodots is crucial for III–V VLS-NW growth [5, 6, 35–37], for hard mask fabrication [27], and plasmonic arrays on insulating and transparent substrates. Fabrication of Au nanodots followed the method described in section 3.2. Resulting in a hexagonal array of 140 nm diameter Au nanodots (figure 4(e)) that completelly covers a 4” silica wafer (figure 4(f)). This result is difficult to obtain by any other nanolithography technique due to the combination of small size (140 nm), large area coverage (4”), and insulating substrate (silica).

4. Conclusions

In summary, PMGI can work as a non-imageable DBARC, resulting in a direct transfer of the nanopattern during the development step which in turn results in a reduction of the nanohole diameter. In addition, PMGI is a lift-off resist that produces an undercut, so, there is no need of an additional lift-off resist layer (LOR). Thus, also simplifying the lift-off process. Moreover, we demonstrate the huge potential of Displacement Talbot Lithography for wafer-scale nanofabrication for several applications as a fast, robust and scalable process. In particular, we have demonstrated the successful substitution of BARC layer by PMGI polymer.

It is worth highlighting that thanks to this innovation we can fabricate nanoholes in a dielectric layer (SiO_2 and SiN_x) with a diameter below 100 nm. The use of a PMGI-based coating in combination with DTL allows a reduction of process complexity by avoiding the use of O_2 plasma etching; both for pattern transfer and for creation of a suitable undercut profile in one step together with resist development. This complexity reduction brings an additional benefit because of the low selectivity between DUV resist and BARC layer against O_2-plasma etching which increases the nanohole size, affects the total thickness of the nanopatterned resists, and creates a nanohole edge slope not optimum for nanohole fabrication. In addition, with only one mask it is possible to select the final size of nanoholes or nanodots in a broad range (from 95 to 200 nm). Therefore, DTL is the perfect candidate for patterning of regular arrays of nanoholes at wafer-scale with a lower fabrication cost than other techniques. This process simplification is also of great importance to the fabrication of nanodots by means of lift-off.

Moreover, the possibilities opened by the PMGI-based coating are illustrated by the successful fabrication of an array of nanoholes with 95 nm diameter for GaAs nanowire growth on a 2″ GaAs wafer, a 2″ nanoimprint lithography (NIL) master stamp, and an array of Au nanodots made by lift-off on a 4″ silica wafer. Therefore, DTL possess the potential for wafer-scale manufacturing of nano-engineered materials. This process can be extended up to 8″ and 12″ wafers. However, there are some practical limitations in the light source, quality of the mirror and of the collimation system, and the quality of the phase shift mask with the regular pattern.

This dynamic exposure process is based on the movement of the substrate perpendicular to the mask, in the 3D diffraction self-image of the regular mask. The yield is limited by the quality of the mask and the beam. The quality of the mask is defined in terms of pattern stitching, pattern size tolerances, homogenous phase shift distribution and the quality of the beam in terms of collimation, and intensity distribution. It is worth mentioning that resist and dielectric thickness variations can affect the homogeneity of the resulting nanopattern as well.

Acknowledgments

Financial support was received from the Knut and Alice Wallenberg Foundation (KAW), the Swedish Research Council (VR), Myfab and NanoLund. This work has been partly supported by the Swedish Foundation for Strategic Research (SSF), within project 'Development of Nanoimprint Infrastructure at Lund Nano Lab as a Key Enabler for Large-Scale Applications of Nanowires', project number RIF14-0090. V J G thanks Dr P A Shields and his group for scientific support and trainning. The authors thank B. Heidari (OpTool AB, Sweden) for supplying GMN-PS90 polymer foils.

Conflicts of interest

The authors declare no competing financial interest.

ORCID iDs

Víctor J Gómez https://orcid.org/0000-0003-2364-8814
Reza Jafari Jam https://orcid.org/0000-0001-9131-0271

References

[1] Wagner C and Harned N 2010 Lithography gets extreme *Nat. Photonics.* **4** 24–26
[2] Tallents G, Wagenaars E and Pert G 2010 Lithography at EUV wavelengths *Nat. Photonics.* **4** 809–11
[3] Vieu C, Carcenac F, Pépin A, Chen Y, Mejias M, Lebib A, Manin-Ferlazzo L, Couraud L and Launois H 2000 Electron beam lithography: resolution limits and applications *Appl. Surf. Sci.* **164** 111–17
[4] Haas F, Sladek K, Winden A, Von Der Ahe M, Weirich T E, Rieger T, Lüth H, Grützmacher D, Schäpers T and Hardtdegen H 2013 Nanoimprint and selective-area MOVPE for growth of GaAs/InAs core/shell nanowires *Nanotechnology* **24** 085603
[5] Jafari Jam R, Heurlin M, Jain V, Kvennefors A, Graczyk M, Maximov I, Borgström M T, Pettersson H and Samuelson L 2015 III-V nanowire synthesis by use of electrodeposited gold particles *Nano Lett.* **15** 134–8
[6] Otnes G, Heurlin M, Graczyk M, Wallentin J, Jacobsson D, Berg A, Maximov I and Borgström M T 2017 Erratum to: strategies to obtain pattern fidelity in nanowire growth from large-area surfaces patterned using nanoimprint lithography (Nano Research, (2016), 9, 10, (2852-2861), 10.1007/s12274-016-1165-z) *Nano Res.* **10** 729
[7] Traub M C, Longsine W and Truskett V N 2016 Advances in Nanoimprint Lithography *Annu. Rev. Chem. Biomol. Eng.* **7** 583–604
[8] Qiao S Z, Liu J and Max Lu G Q 2017 *Synthetic Chemistry of Nanomaterials* (Amsterdam: Elsevier) pp 613–40
[9] Colson P, Henrist C and Cloots R 2013 Nanosphere lithography: A powerful method for the controlled manufacturing of nanomaterials *J. Nanomater.* **2013** 948510
[10] Lu C and Lipson R H 2010 Interference lithography: a powerful tool for fabricating periodic structures *Laser Photonics Rev.* **4** 568–80
[11] Isoyan A, Jiang F, Cheng Y C, Cerrina F, Wachulak P, Urbanski L, Rocca J, Menoni C and Marconi M 2009 Talbot lithography: self-imaging of complex structures *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **27** 2931–7
[12] Yuan X C, Zhang D G, Sun Y Y, Bu J and Zhu S W 2009 Fabrication of three-dimensional photonic crystals with the Talbot self-imaging effect *J. Opt. A Pure Appl. Opt.* **11** 105104
[13] Stuerzebecher L, Harzendorf T, Vogler U, Zeitner U D and Voelkel R 2010 Advanced mask aligner lithography: fabrication of periodic patterns using pinhole array mask and Talbot effect *Opt. Express* **18** 19485
[14] Chausse P J P, Le Boulbar E D, Lis S D and Shields P A 2019 Understanding resolution limit of displacement Talbot lithography *Opt. Express.* **27** 5918
[15] Solak H H, Dais C and Clube F 2011 Displacement Talbot lithography: a new method for high-resolution patterning of large areas *Opt. Express.* **19** 10686
[16] Solak H H, Dais C, Clube F and Wang L 2015 Phase shifting masks in Displacement Talbot Lithography for printing nano-grids and periodic motifs *Microelectron. Eng.* **143** 74–80
[17] Wang L, Clube F, Dais C, Solak H H and Gobrecht J 2016 Sub-wavelength printing in the deep ultra-violet region using Displacement Talbot Lithography *Microelectron. Eng.* **161** 104–8

[18] Le Boulbar E D, Chausse P J P, Lis S and Shields P A 2017 Displacement Talbot lithography: an alternative technique to fabricate nanostructured metamaterials *Proc. SPIE* **10248** 102480Q
[19] Coulon P-M *et al* 2017 Optical properties and resonant cavity modes in axial InGaN/GaN nanotube microcavities *Opt. Express.* **25** 28246
[20] Coulon P M, Kusch G, Le Boulbar E D, Chausse P, Bryce C, Martin R W and Shields P A 2018 Hybrid top-down/bottom-up fabrication of regular arrays of AlN nanorods for Deep-UV Core–Shell LEDs *Phys. Status Solidi Basic Res.* **255** 1700445
[21] Coulon P M, Kusch G, Fletcher P, Chausse P, Martin R W and Shields P A 2018 Hybrid top-down/bottom-up fabrication of a highly uniform and organized faceted AlN nanorod scaffold *Materials* **11** 1140
[22] Damilano B, Coulon P M, Vézian S, Brändli V, Duboz J Y, Massies J and Shields P A 2019 Top-down fabrication of GaN nano-laser arrays by displacement Talbot lithography and selective area sublimation *Appl. Phys. Express.* **12** 10–15
[23] Le-The H, Berenschot E, Tiggelaar R M, Tas N R, van den Berg A and Eijkel J C T 2017 Shrinkage control of photoresist for large-area fabrication of Sub-30 nm periodic nanocolumns *Adv. Mater. Technol.* **2** 1600238
[24] Lee C-S, Lee -Y-Y, Chong K S L, Wang L, Dais C, Clube F, Solak H H, Mohacsi I, David C and Bischofberger R 2016 High-resolution, high-aspect-ratio iridium–nickel composite nanoimprint molds *J. Vac. Sci. Technol. B* **34** 061804
[25] Xie S, Schurink B, Berenschot E J W, Tiggelaar R M, Gardeniers H J G E and Luttge R 2016 Displacement Talbot lithography nanopatterned microsieve array for directional neuronal network formation in brain-on-chip *J. Vac. Sci. Technol. B* **34** 06KI02
[26] Chausse P, Le Boulbar E D, Coulon P and Shields P A 2019 'Double' displacement Talbot lithography: fast, wafer-scale, direct-writing of complex periodic nanopatterns *Opt. Express* **27** 32037–46
[27] Coulon P-M *et al* 2019 Displacement Talbot Lithography for nano-engineering of III-nitride materials *Microsyst. Nanoeng.* **5** 52
[28] Hwang S H, Lee K K and Jung J C 2000 A novel organic bottom anti-reflective coating material for 193 nm excimer laser lithography *Polymer (Guildf)* **41** 6691–4
[29] Kudo T *et al* 2010 Advances and challenges in developable bottom anti-reflective coating (DBARC) *J. Photopolym. Sci. Technol.* **23** 731–40
[30] Kudo T *et al* 2009 Latest developments in photosensitive developable bottom anti-reflective coating. (DBARC) *Proc. SPIE* **7520** 75200N
[31] Hatanaka T, Kimura S, Enomoto T and Nakajima Y 2004 Wet developable bottom antireflective coatings *Proc. SPIE* **5376** 655
[32] Roh H J, Ju D K, Kim H J and Kim J 2011 Study of major factors to affect photoresist profile on developable bottom anti-reflective coating process *Proc. SPIE* **7972** 79721Q
[33] Toukhy M, Oberlander J, Mullen S, Lu P and Neisser M 2007 Radiation sensitive developable bottom anti-reflective coatings (DBARC) for 193nm lithography: first generation *Proc. SPIE* **6519** 651936
[34] Brewer Science Inc. 2010. Brewer Science GenARC 266 Coating 1–2 (https://www.brewerscience.com/products/arc/)
[35] Barrigón E, Heurlin M, Bi Z, Monemar B and Samuelson L 2019 Synthesis and applications of III–V nanowires *Chem. Rev.* **119** 9170–220
[36] Albert S, Bengoechea-Encabo A, Sánchez-García M A, Kong X, Trampert A and Calleja E 2013 Selective area growth of In(Ga)N/GaN nanocolumns by molecular beam epitaxy on GaN-buffered Si(111): from ultraviolet to infrared emission *Nanotechnology* **24** 175303
[37] Russo-Averchi E *et al* 2015 High yield of gaas nanowire arrays on si mediated by the pinning and contact angle of Ga *Nano Lett.* **15** 2869–74
[38] Doemling M F, Rueger N R, Oehrlein G S and Cook J M 1998 Photoresist erosion studied in an inductively coupled plasma reactor employing CHF3 *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **16** 1998–2005
[39] Microchem Corp. 2015. LOR and PMGI Resists (https://kayakuam.com/wp-content/uploads/2019/09/PMGI-Resists-data-sheetV-rhcedit-102206.pdf)
[40] Eriksson T, Yamada S, Venkatesh Krishnan P, Ramasamy S and Heidari B 2011 High volume nanoimprint lithography on III/V substrates: imprint fidelity and stamp lifetime *Microelectron. Eng.* **88** 293–9